C-Band 10 W MMIC Class-A Amplifier Manufactured Using the Refractory SAG Process

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Abstract—**This paper describes the design, fabrication, and test results of a *C*-Band single-chip GaAs MMIC class-A amplifier manufactured using the ITT multifunctional self-aligned gate (MSAG) process. The amplifier demonstrates a 10 W power output (0.625 W/mm power density) at 5.5 GHz with an associated gain of 5 dB and a power-added efficiency of 36 percent. The average functional yield of the IC was above 70 percent. To our knowledge, these results exceed the best published results for *C*-band power MMIC amplifiers.**

I. Introduction

THERE IS A great deal of interest in finding more reliable power sources for wide-band communication, T/R modules, and ECM applications. Power MMIC amplifiers using MESFET technology look very attractive in terms of cost, weight, reproducibility, and reliability and offer lower power supply voltages. Although there are fundamental limitations on the power that can be generated from a single discrete FET, achievable power levels can be significantly increased by combining a number of FET's on a single GaAs chip amplifier. These chips can be further combined using standard hybrid MIC techniques to obtain much higher power levels.

During the past decade there has been significant progress in monolithic power amplifiers covering narrow-band and broad-band frequency ranges [1]–[10]. Power levels of 6 W from a single MMIC chip at *C*-band have been reported. At ITT/GTC we have developed MMIC power amplifiers using a new fully planar, multifunctional self-aligned gate (MSAG) technology [11] demonstrating state-of-the-art performance in a manufacturing environment. This paper reports the design, fabrication, and test results of a *C*-band single-chip MMIC power amplifier with 10 W power output (0.625 W/mm power density), 36 percent power-added efficiency, and 0.54 W/mm^2 power density for the chip area.

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II. Power FET Design

The design of a high-power MMIC amplifier starts with the design of the power MESFET. The input impedance level, the heat dissipation, the source inductance, and the phase difference between different parts of the power FET play a significant role in the selection of FET size. In the current design we have used a 4 mm gate periphery FET which is optimized for maximum power and efficiency at *C*-band by reducing the source series resistance (R_s) and the thermal resistance (R_{th}). The electrode dimensions are as follows: the source–drain ohmic metal spacing is 10 μm; the drain n^+ edge is 1.6 μm from the gate center; the source fingers are 46 μm long (dimension perpendicular to the gate width); the drain fingers are 34 μm long; the gate Schottky contact is 0.5 μm long and has an 0.8-μm-long gold overlay; and the gate electrode center is 2.0 μm from the source finger. This results in a constant 50 μm separation between the 16 gate fingers which constitute one cell. The gate fingers are 250 μm wide. The large gate–drain spacing was used to increase the breakdown voltage for catastrophic failure between these electrodes. The 4 mm FET as shown in Fig. 1 has three source vias for low parasitic source grounding (0.05 Ω, 0.01 nH for each via typically). The substrate thickness, 75 μm, is chosen as a compromise between reducing R_{th} and being able to design and handle power MMIC's.

Thermal analysis of ITT/GTC power FET's was performed utilizing a Barnes IR imager. The thermal impedance (θ_j) was measured to be about 20°C/W for 2.5 mm gate periphery devices on a 75-μm-thick substrate. The estimated value for the 4 mm pair device is about 7°C/W. The average channel temperature (T_{ch}) of the device under RF operation may be calculated using the following relation:

$$T_{ch} = \left[P_{dc} + P_{in}(\mathrm{RF}) - P_o(\mathrm{RF})\right]\theta_j + T_{case} \qquad \text{(i)}$$

where P_{dc}, P_{in} and P_o are the dc power dissipated, the RF power into the device, and the RF power out of the device, respectively. Rearranging this equation in terms of power

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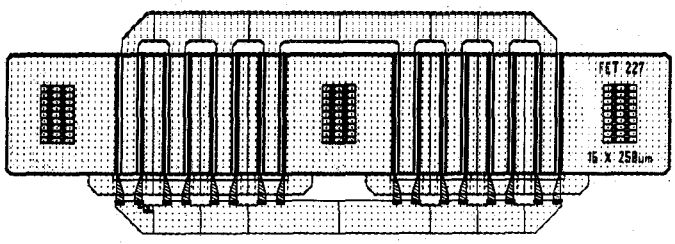

Fig. 1. CALMA layout of the 4 mm FET.

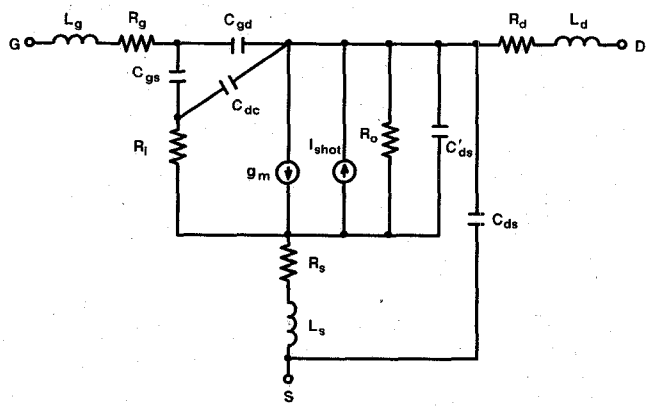

Fig. 2. Equivalent circuit model of a power FET.

gain ($G = P_o/P_{in}$) and power-added efficiency ($\eta_{add} = (P_o - P_{in})/P_{dc}$),

$$T_{ch} = P_o\left(1-\frac{1}{G}\right)\left(\frac{1}{\eta_{add}}-1\right)\theta_j + T_{case}. \qquad \text{(ii)}$$

In the 10 W amplifier (having two 4 mm pairs) if each 4 mm FET pair has a power out of 5.5 W, a gain of 5.5 dB, an efficiency of 38 percent, and a case temperature of 42°C (measured with heat sink), the channel temperature is calculated to be approximately 87°C, which is low enough to ensure reliable operation.

III. Power FET Model

The power amplifier design reported here is based on an innovative method for modeling the power characteristics of FET's which was developed at the ITT Gallium Arsenide Technology Center. The method determines accurate linear models for power FET's which are used to design matching networks and to simulate accurately the performance of power amplifiers. The method is suitable for single and multistage amplifiers. The models are derived by measuring I–V characteristics, small-signal S parameters measured at 3, 25 and 40 percent of I_{DSS}, and load-pull contour data at the operating drain–source voltage and frequencies. The procedure used to derive the linear model for the power FET's is described briefly in the following.

i) Determine small-signal lumped element values for a FET model as shown in Fig. 2 from measured S parameters. The nonlinear elements are C_{gs}, C_{gd}, g_m, and R_o.

ii) Determine the optimum source reflection coefficient Γ_S^* and the load reflection coefficient Γ_L^* from measured load-pull data for maximum power output at $P_{1\,dB}$.

iii) Change slightly C_{gs} and C_{gd}, and select R_o as $R_o^L \simeq 1/3$ to $1/5$ of the small-signal value of R_o to fit Γ_S^* and Γ_L^*. This model is suitable for designing input and output matching networks.

iv) Now use the model derived in step (iii) and modify g_m and R_o^L ($\simeq 1/2$ of the small-signal value of R_o derived in step (i)) to adjust the gain obtained in step (ii) as $G_{1\,dB}$ when the source impedance Z_S^* and the load impedance Z_L^* are connected to the FET. This model will be used to calculate the IC performance.

TABLE I
Typical Equivalent Circuit Model Values for a 4 mm FET

	Parameter	Value
L_g	(gate inductance)	0.05 nH
L_s	(source inductance)	0.02 nH
L_d	(drain inductance)	0.05 nH
R_g	(gate ohmic resistance)	0.6 Ω
R_s	(source bulk resistance)	0.4 Ω
R_d	(drain bulk resistance)	0.4 Ω
R_i	(channel resistance)	0.6 Ω
R_o	(drain to source resistance for performance calculation)	20 Ω
R_o	(for matching to load line)	13 Ω
C_{gs}	(gate-to-source capacitance)	5.0 pF
C_{gd}	(gate-to-drain capacitance)	0.064 pF
C_{dc}	(dipole capacitance)	0.032 pF
C'_{ds}	(drain-to-source capacitance)	0.96 pF
C_{ds}	(drain-to-ground capacitance)	0.112 pF
g_m	(transconductance)	300 mS
t	(transit time)	3.0 ps

The equivalent circuit of a power FET is shown in Fig. 2, and the element values are given in Table I. Typical measured performance for the discrete 4 mm FET at 1 dB compression point includes 7 dB gain, 40 percent power-added efficiency, and 3.0 W power output at 5.5 GHz. The FET's are operated at V_{DS} of 8.5 V and $I_{DS} = 40$ percent of I_{DSS} (I_{DSS} for 4 mm FET is about 1500 mA).

IV. Circuit Design

In order to meet our objectives of 8 W power output with reasonably good MIC yield, two single-ended amplifiers with outputs combined on a single chip were used to achieve the high power output. Each of the single-ended amplifiers used a pair of reactively combined standard 4 mm gate FET's for a net 8 mm of FET gate periphery.

Each 8 mm FET periphery is matched to 100 Ω input and output under maximum power output condition. Both distributed and lumped elements were used in the matching networks. The elements of the output matching network were selected for minimum possible loss with a good match as well as to satisfy electromigration requirements (maximum allowed current density in the bias lines was 2×10^5 A/cm^2). Finally, two of these single-ended designs were combined on chip to complete the 8 W amplifier.

The capacitors used for dc blocking, RF bypassing, and matching were all of the metal–insulator–metal (MIM)

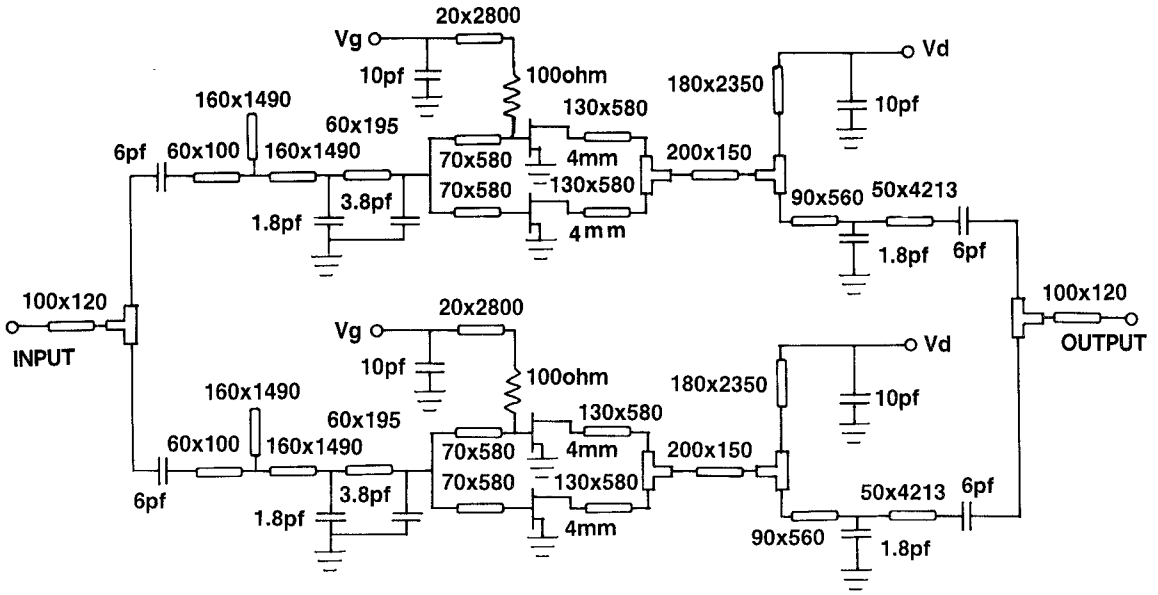

Fig. 3. Schematic of a 10 W power amplifier.

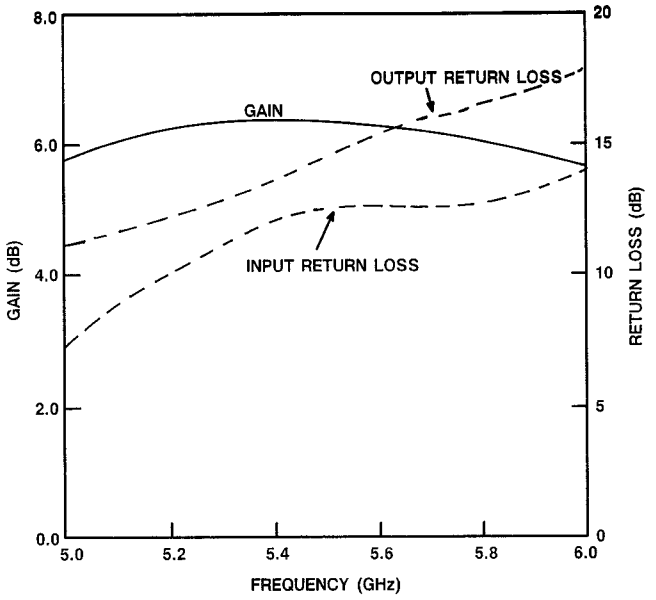

Fig. 4. Simulated performance of the high-power MMIC chip.

type. The dielectric material used for the capacitor is 2000-Å-thick Si_3N_4. This provides a capacitance of 300 pF/mm^2 and a breakdown voltage of above 30 V. The tolerance in capacitance is ± 5 percent. Large RF bypass capacitors as well as resistive gate bias were used for low-frequency amplifier stabilization. The drain bias is applied to each FET through a low-impedance short-circuited stub. Fig. 3 shows a schematic diagram of the 8 W power amplifier chip with simulated performance shown in Fig. 4.

The sensitivity of power amplifiers was investigated with respect to four process parameters: C_{gs} (± 10 percent), g_m (± 10 percent), R_o (± 10 percent), and MIM capacitors (± 5 percent). The analysis was carried out using Monte Carlo simulation (EEsof Inc.). The pass–fail criterion was 6 dB minimum gain over the 5.2 to 5.8 frequency range. After 200 trials the pass percentage was 68 percent. Of these four parameters only g_m demonstrated significant effect on the performance.

V. Fabrication

The power IC's reported in this paper were fabricated using the refractory metal, multifunctional self-aligned gate (MSAG) MMIC process developed at ITT/GTC. A detailed description of the process is given in [11]. Some of the key features of the process are as follows:

- Since the FET I_{DSS} is determined by implantation rather than gate recess, I_{DSS} uniformity is remarkably improved. Typical uniformity is better than 5 percent.
- Gate–source resistance is minimized using an n^+ implant which self-aligns to the gate. FET performance is reasonably insensitive to gate location, resulting in excellent photolithography tolerance.
- The Schottky metal is titanium tungsten nitride (TiWN), an extremely good gold diffusion barrier. Given that the Schottky survives an 825°C anneal, it is unlikely to fail at less than 300°C.
- The gate parasitic resistance is reduced to a very low level using gold overlay metal, which is isolated from the GaAs surface by silicon nitride dielectric and the TiWN Schottky.
- The n^+ and the drain electrode on the drain side are moved away from the gate to maintain high gate–drain breakdown voltage and high output resistance.

The process includes Au/Ge/Ni metallization for ohmic contacts, 0.5 μm TiWN Schottky barrier gates, and ion-implanted resistors. The 0.5 μm TiWN gates are covered by a 0.8 μm overlay, after planarization. Silicon nitride is used for both capacitors and passivation. The air bridges, microstrip lines, and bonding pads are 5-μm-thick plated

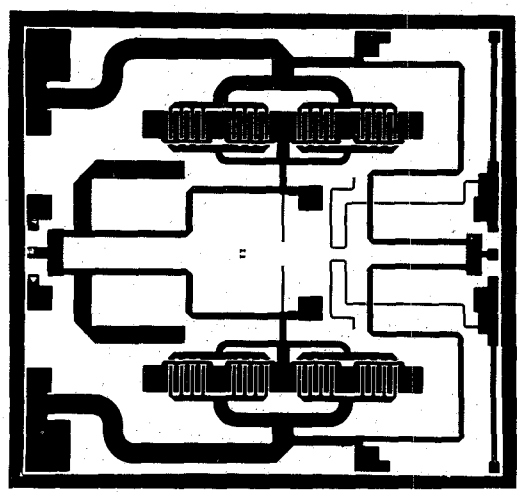

Fig. 5. Photograph of a 10 W power MMIC. (Chip size = 4.14×4.48×0.075 mm^3)

TABLE II
SUMMARY OF RF FUNCTIONAL YIELD OF 10 W POWER IC'S

Lot #	End-of-Process Wafer Yield (%)	IC Yield — Wafer Number 1	2	3	4	5	6	Average IC Yield in a Lot (%)
1	67	81	--	62	--	63	81	72
2	83	68	81	78	59	78	--	73
3	67	72	62	86	--	--	81	75

gold. The wafer is lapped to its final thickness of 75 μm, and back side via holes are then etched and plated. A photograph of the chip is shown in Fig. 5.

VI. Test Results

Table II gives a summary by lot of the RF functional "on-wafer" yield. This is a low-power screening test. Each lot originally contains six 3-in-diameter wafers. For RF functional yield the devices are biased at $V_{DS} = 3$ V and $V_{GS} = -4$ V (near pinch-off). The average measured functional yield for three lots was above 70 percent.

Several 8 W amplifiers were assembled on a 0.5×0.5 in^2 gold-plated Elkonite (Cu–W) carrier for RF characterization. Elkonite material was chosen for good thermal conductivity and thermal expansion match to GaAs and alumina. The carrier 50 Ω microstrip lines are printed on 250 μm (10 mil) thick alumina substrate. Although IC's were fabricated on a thin substrate (75 μm thick) using 18 via holes, we had no problem in assembling these chips using gold–tin (AuSn) die attach at 290°C.

Typical measured characteristics for the IC are plotted in Fig. 6 as a function of input power at 5.5 GHz. The amplifier has about 6 dB gain, 9 W power output, and 37 percent power-added efficiency at the 1 dB gain compression point. At the 2 dB gain compression point the peak power output was 10 W (0.63 W/mm power density for 4 mm FET's) and 38 percent power-added efficiency. The power output for the chip was 0.54 W/mm^2, which is the highest power density per unit chip area at *C*-band reported so far. Power out as a function of frequency at 1 dB gain compression is shown in Fig. 7. The gain flatness is ±0.5 dB over the 5.2 to 6 GHz frequency range.

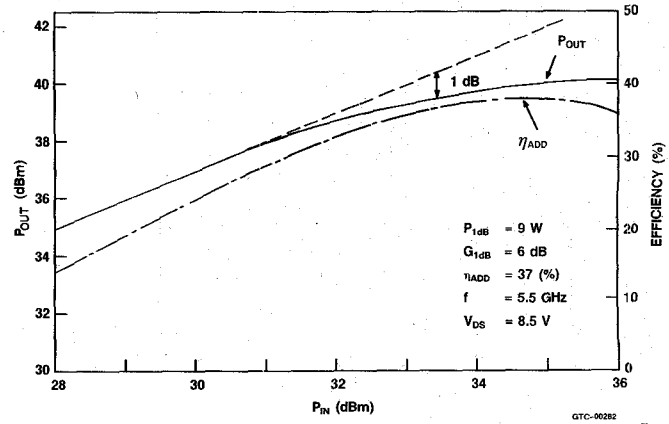

Fig. 6. Power output versus power input for a 10 W power MMIC.

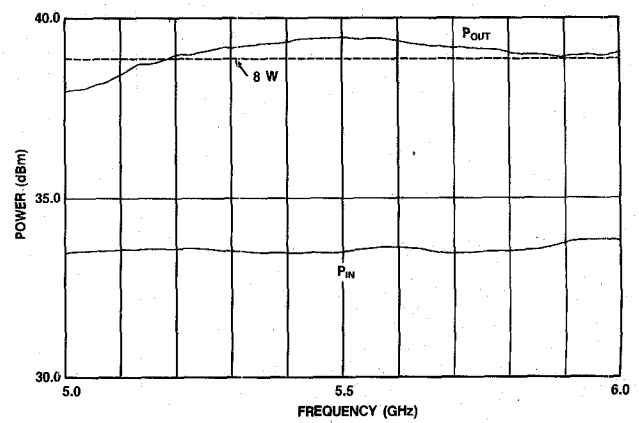

Fig. 7. Variation of P_{out} and P_{in} as a function of frequency of a 10 W power MMIC.

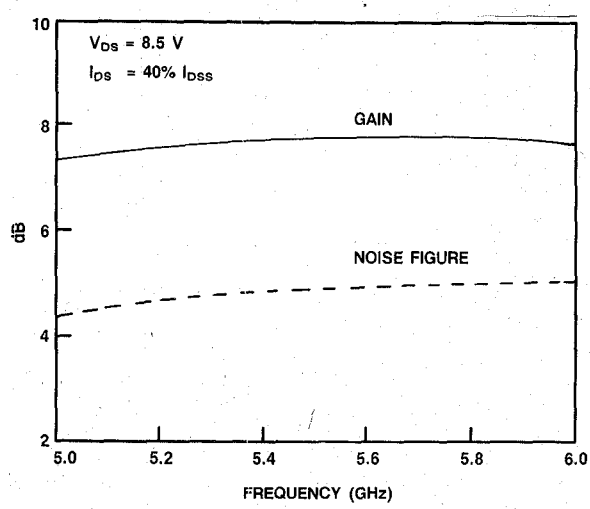

Fig. 8. Measured small-signal performance of the 10 W MMIC chip.

The measured noise figure and small-signal gain of the high-power chip (biased at $V_{DS} = 8.5$ V and $I_{DS} = 40$ percent of I_{DSS}) are shown in Fig. 8. The noise figure was less than 5.2 dB over the 5 to 6 GHz band. The AM to PM conversion was also measured. The transfer phase difference (with respect to $P_{in} = 20$ dBm) as a function of input power is plotted in Fig. 9. The measured AM to PM

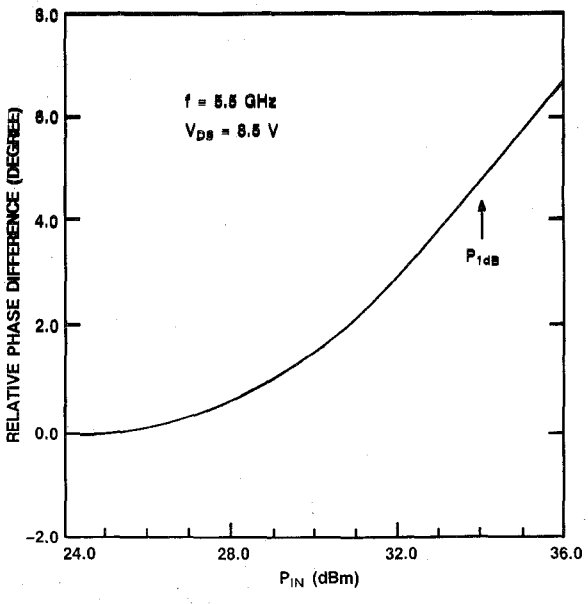

Fig. 9. Measured AM to PM conversion of the 10 W MMIC chip.

TABLE III
SUMMARY OF MEASURED RESULTS FOR 10 W MMIC AMPLIFIERS

Parameter	Goals	Measured
Frequency (GHz)	5.2-5.8	5.2-6.0
P_{1dB} (min)	8.0	8.0
P_{2dB} (min)	8.5	9.0
P_o/mm (W/mm) @P_{2dB}	0.53	0.56
Gain (dB), Min. @P_{1dB}	5.5	5.5
Power Added Efficiency (%), Min. @P_{1dB}	30	32
Noise Figure (dB), Max.	8	5.2
VSWR, Max.	2:1	3:1

conversion at the $P_{1\,dB}$ level was about 1°/dB. Table III summarizes the measured results for these amplifiers.

VII. Conclusions

In summary, we developed a *C*-band 10 W single-chip power MMIC amplifier with 10 W power output (0.625 W/mm) and 36 percent power-added efficiency at 5.5 GHz demonstrating state-of-the-art performance. The power density per unit chip area was 0.54 W/mm^2. This excellent performance is attributed to an accurate model for 4 mm FET's, a new IC design method, simple circuit topology, and high-yield, high-performance MSAG processing.

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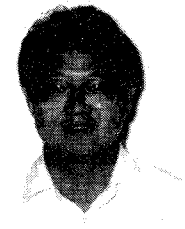
Inder J. Bahl (M'80–SM'80–F'89), for a photograph and a biography, please see page 1320 of the September 1989 issue of this TRANSACTIONS.



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